

DEMONSTRATING BANKABILITY

**Potential-induced degradation testing –
a critical addition to today's qualification tests**

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Primary References

- This presentation is primarily based on a few most recent documents / publications:
 - IEC 62804: System voltage durability qualification test for crystalline silicon modules, DRAFT Sep 2013.
 - Round robin testing: NREL, USA; PI-Berlin, Germany; Fraunhofer ISE, Germany; Fraunhofer CSP, Germany; TÜV Rheinland, Germany, Aug 2013.
 - P. Hacke et al., Development of an IEC test for crystalline silicon modules to qualify their resistance to system voltage stress, EU PVSEC, Sep 2013
 - J. Berghold et al., PID test round robins and outdoor correlation, EU PVSEC, Sep 2013
 - P. Hacke, Considerations for a Standardized Test for Potential-Induced Degradation of Crystalline Silicon PV Modules, PV Module Reliability Workshop, 2012.
 - S. Goranti and G. TamizhMani, Potential Induced Degradation Study on Accelerated Stress Tested PV Modules, IEEE Photovoltaic Specialists Conference, 2012.
 - S. Pingel et al., "Potential Induced Degradation of Solar Cells and Panels," IEEE Photovoltaic Specialists Conference, 2010.

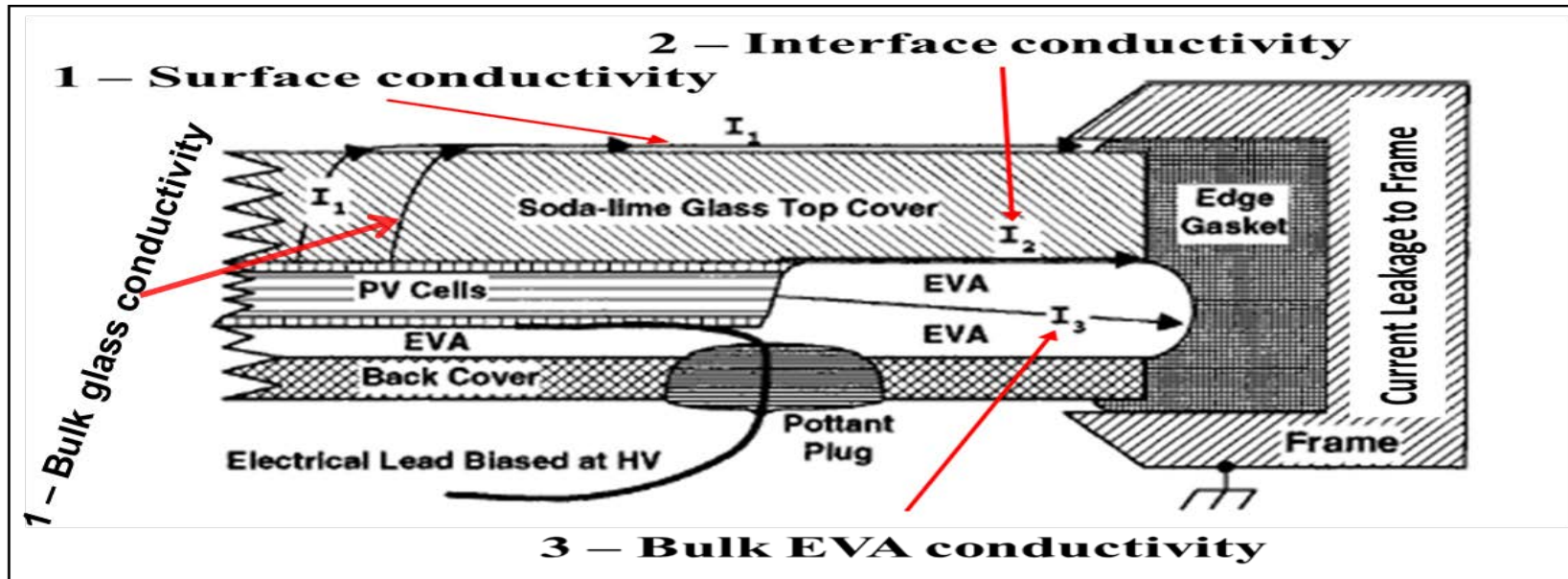
Outline

- **PID**
 - **Background**
 - **Field Observations**
 - **Accelerated Tests and Their Results**
 - **IEC Standard (*Draft*)**
 - **Conclusions**

PID: Background

PID: An electrochemical reaction

Electrochemical reaction: Both electrodes and ionic conductors are involved



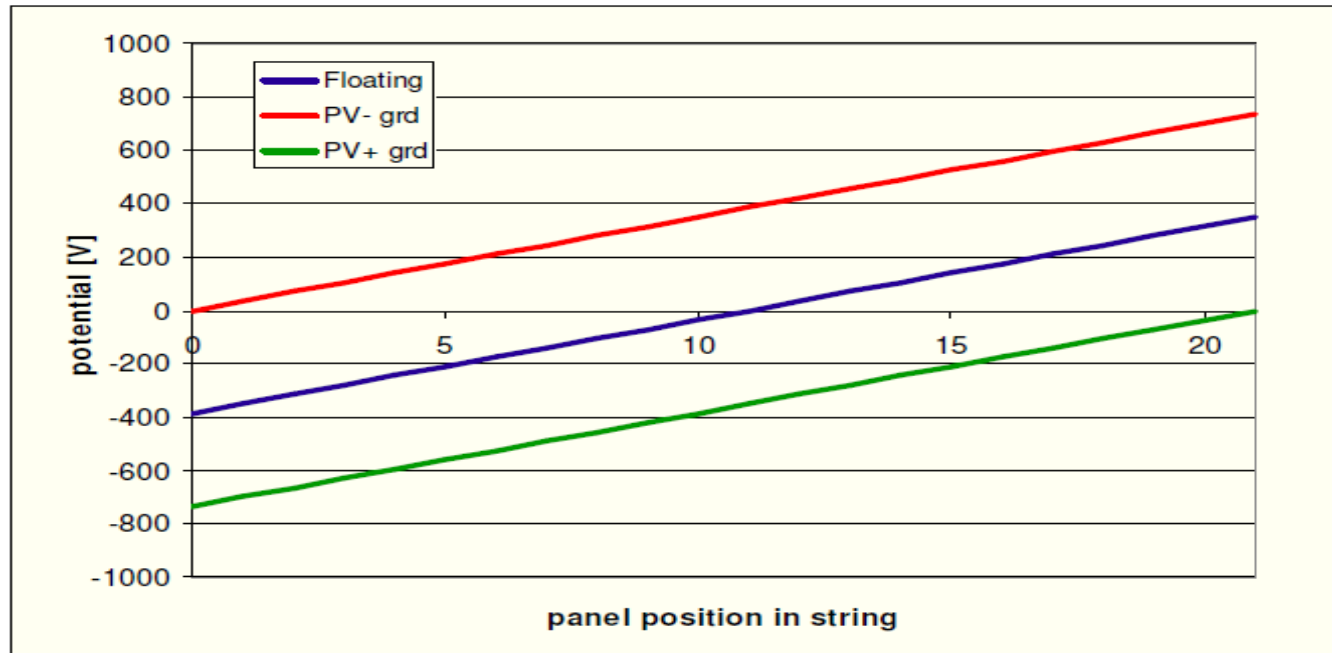
- **Working Electrode:** Cell
- **Counter Electrode:** Metallic frame (or conductive mounting means)
- **Ionic conducting medium:**
 1. Glass-Bulk (Na^+ ions movement at high voltages); Glass-Surface (water layer and/or conductive dirt)
 2. Interface (water layer due to delamination)
 3. EVA-Bulk (moisture absorption due to backskin or edge water vapor transport)

PID: Critical Significance to Sellers and Buyers

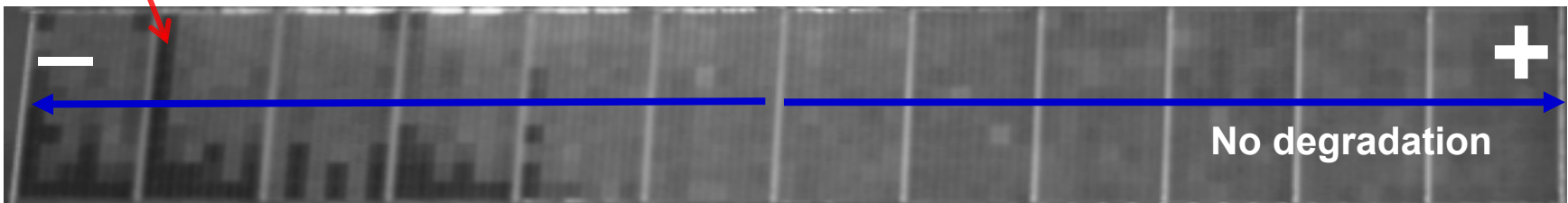
- System voltage can cause degradation of large systems by tens of percent in a single year
- Positive or negative grounded system may experience PID depending on the module/cell type
- In floating systems, the modules are subjected to both positive and negative bias stresses
- PID problem can be solved for conventional modules by adjusting the silicon nitride layer on the cells, by using a high-resistance encapsulant, by adjusting the system voltage level and/or polarity, or by using MLPE (module level power electronics)
- PID susceptibility issue can be easily and quickly detected through a few hours or days of inexpensive tests

PID: Field Observations

PID: Dependence on grounding polarity



Shunted cells near the frame



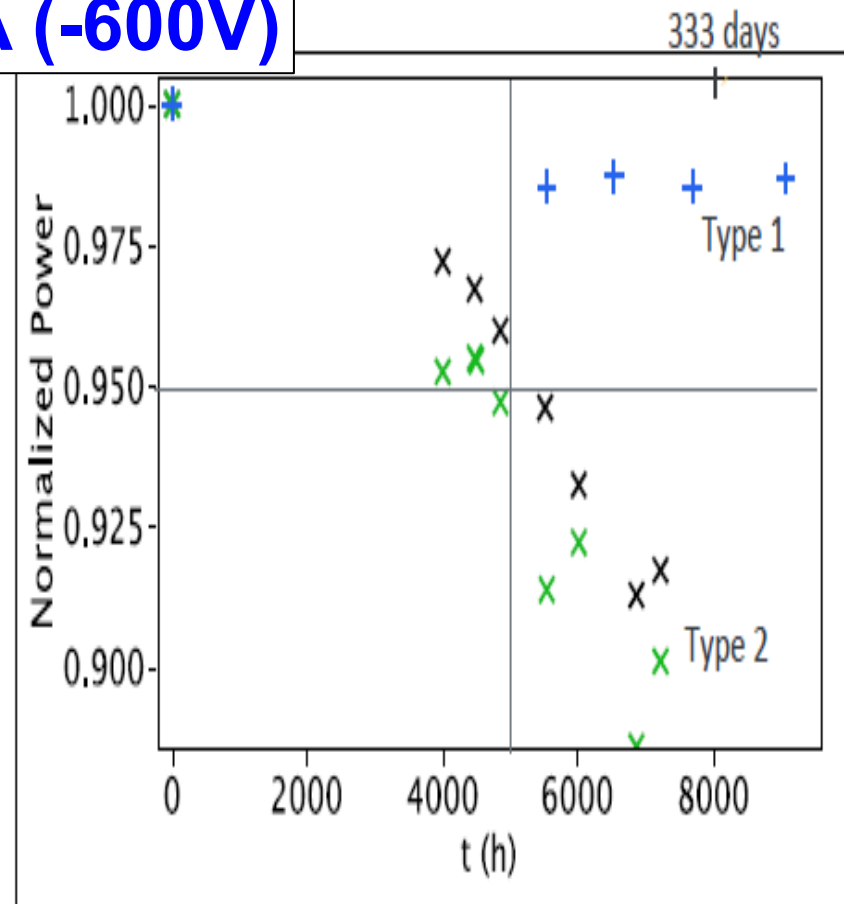
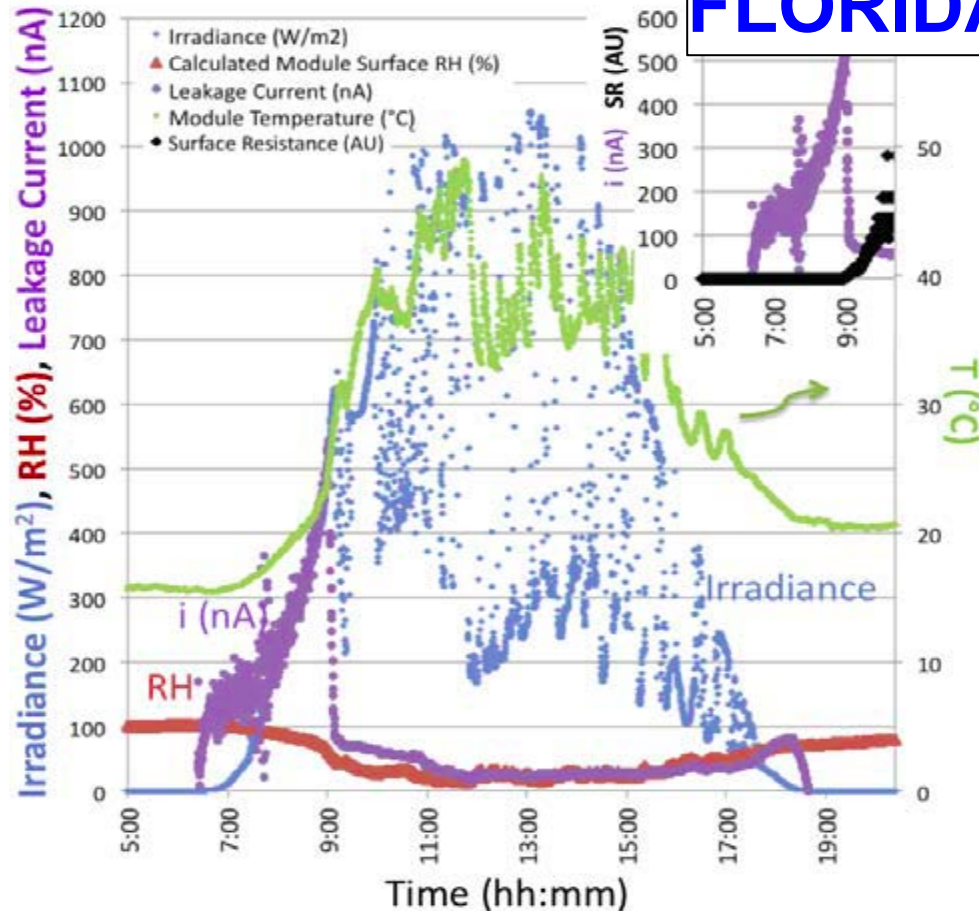
EL Images of a floating string

Bias Polarity:

Degradation dependence is dictated by the bias polarity and level

PID: Dependence on temperature, humidity and module type

FLORIDA (-600V)

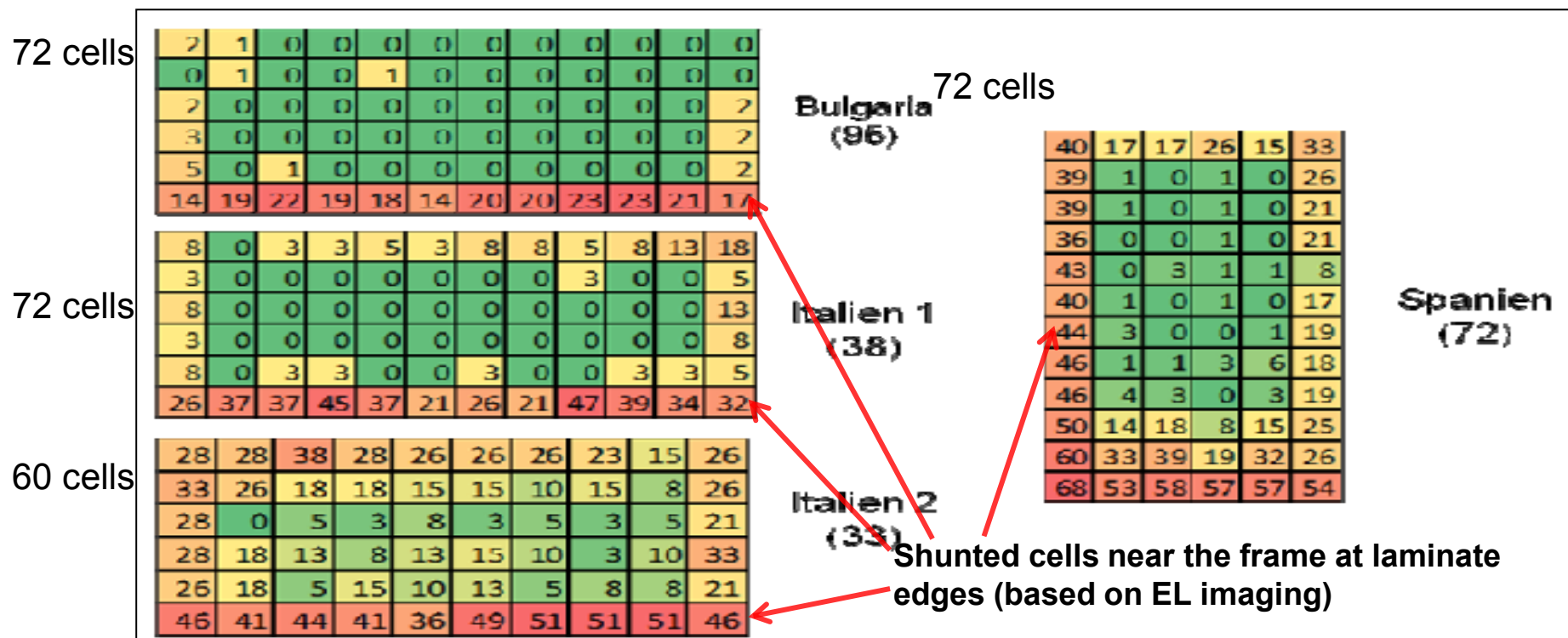


Temperature, Humidity and Type:

Degradation rate is very sensitive to temperature, humidity and module/cell type

PID: Dependence on counter electrode (frame) location

The orientation of the images for the different solar projects is representing the installation situation (landscape versus portrait). The numbers in the images for the different projects are reflecting the percentage of cells being PID affected at this position of the module.

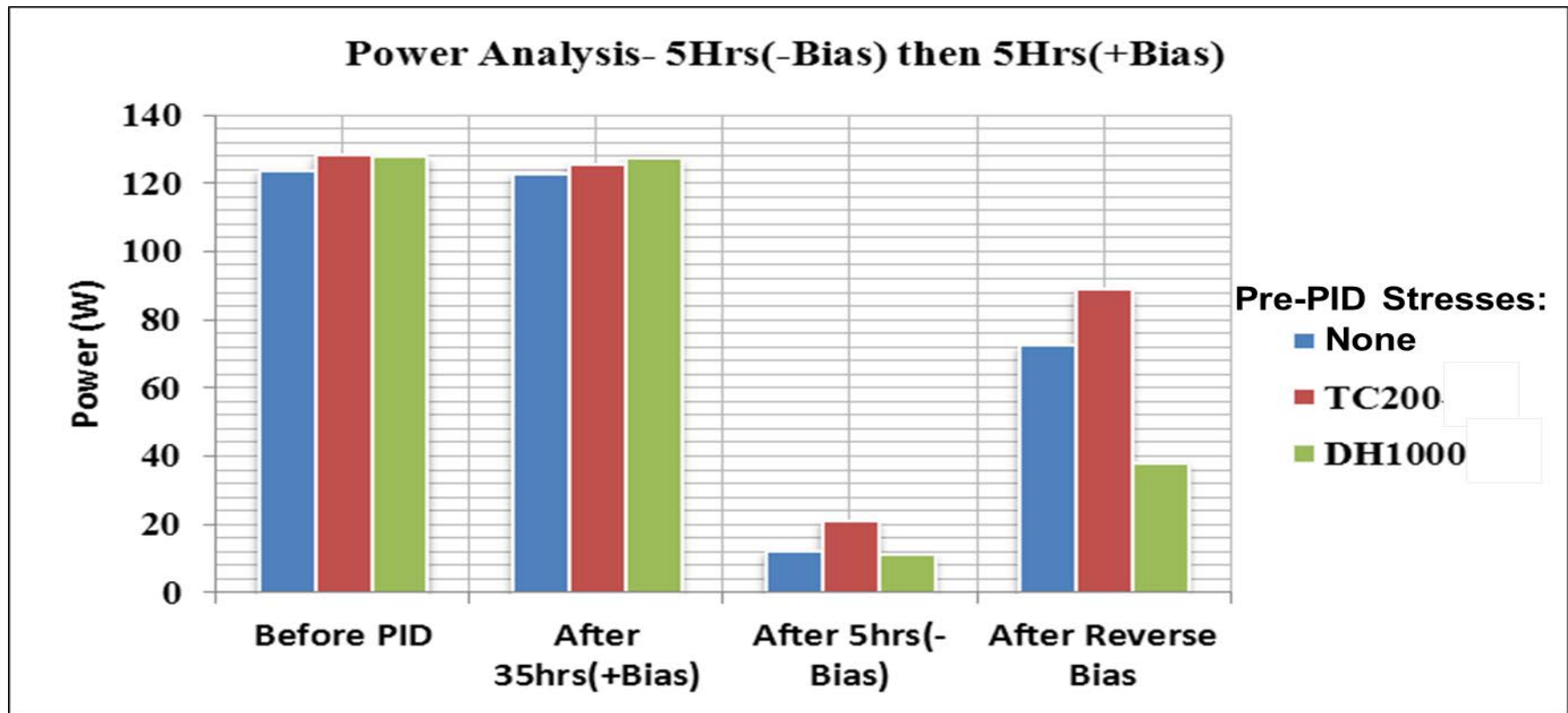


Counter Electrode Location:

Cell degradation **pattern** within a module in field depends on the counter electrode location

PID: Accelerated Tests and Their Results

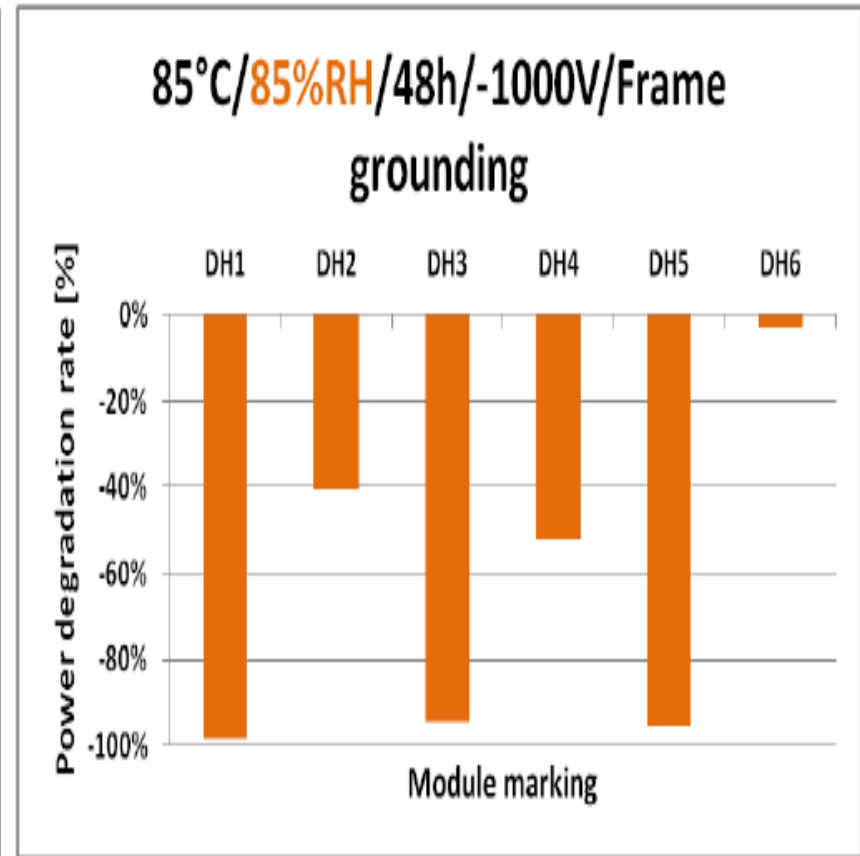
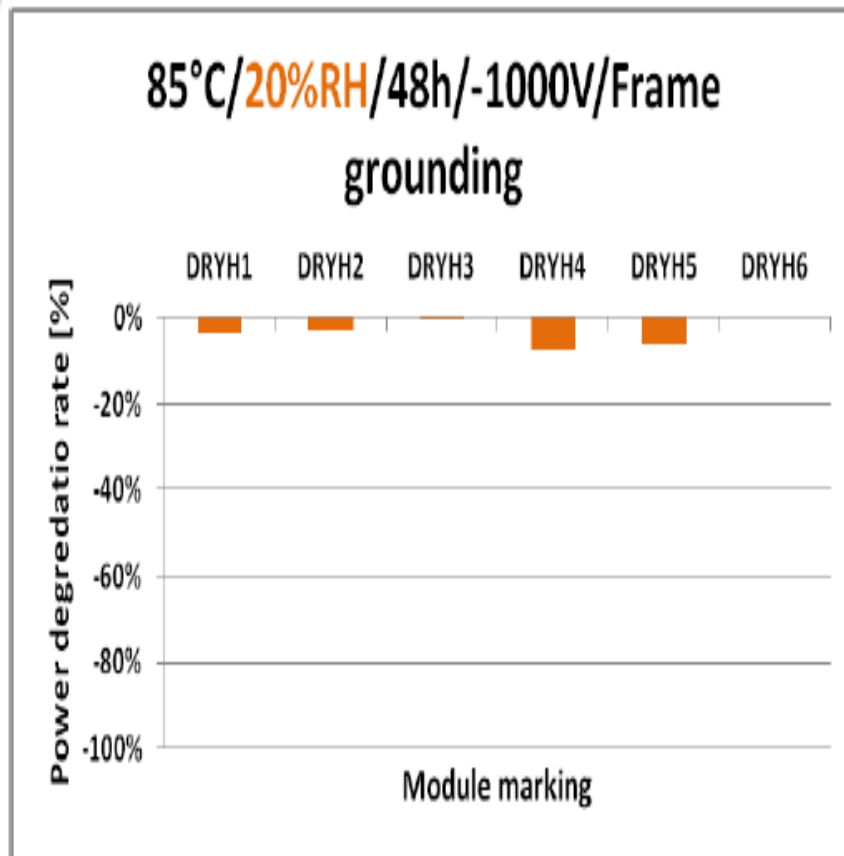
PID: Dependence on grounding polarity



Bias Polarity:

Degradation dependence is dictated by bias polarity
(test at both polarities if no specific polarity specified by manufacturer)

PID: Dependence on humidity

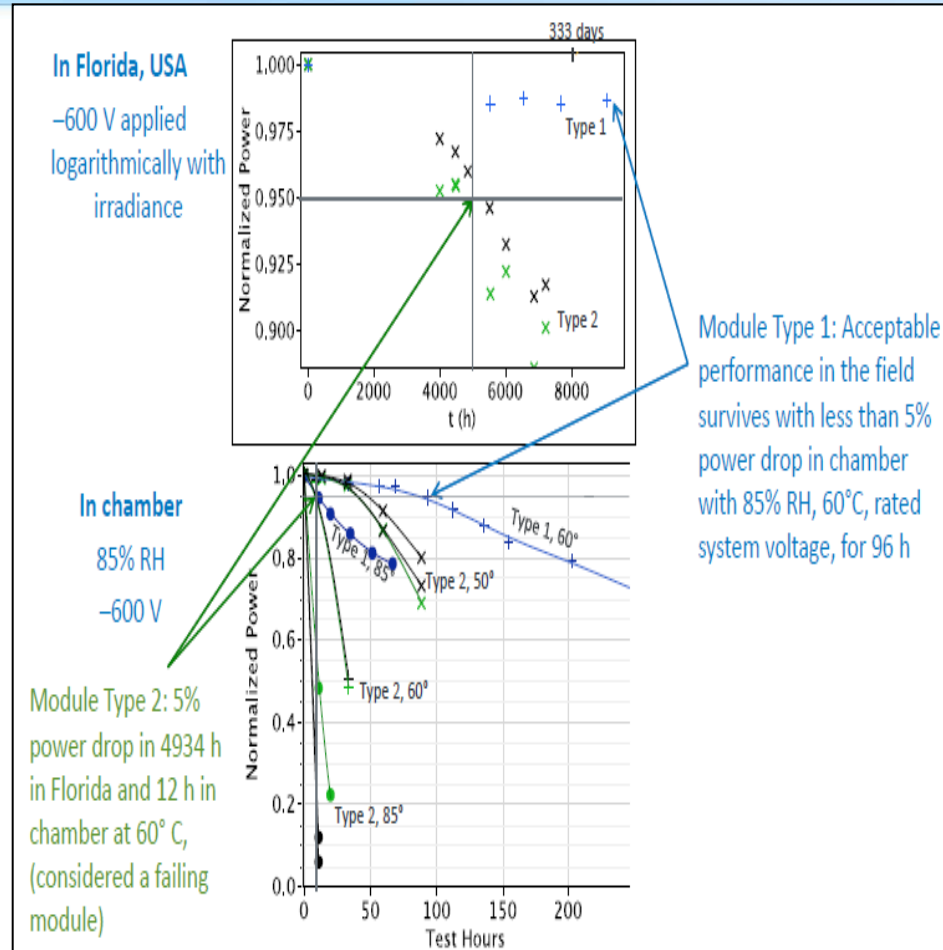
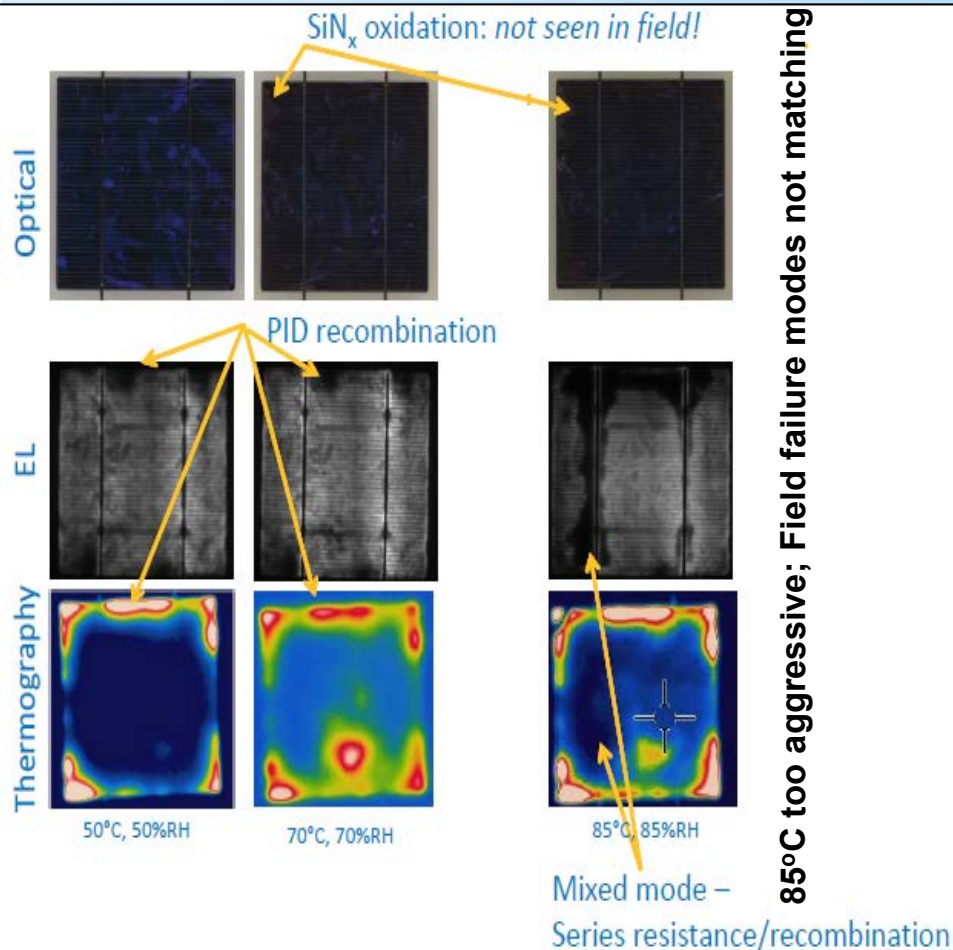


Humidity Level:

Degradation rate is very sensitive to the humidity level and tolerance

(for better repeatability and reproducibility, chamber RH% tolerance needs to be decreased from +/-5% to a lower value)

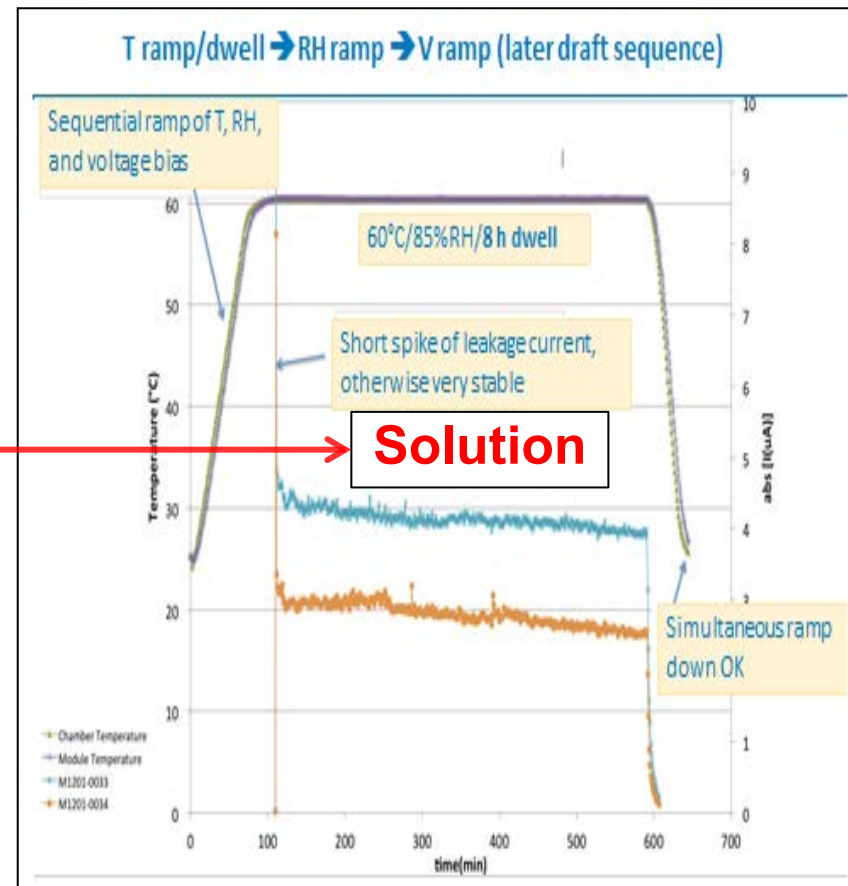
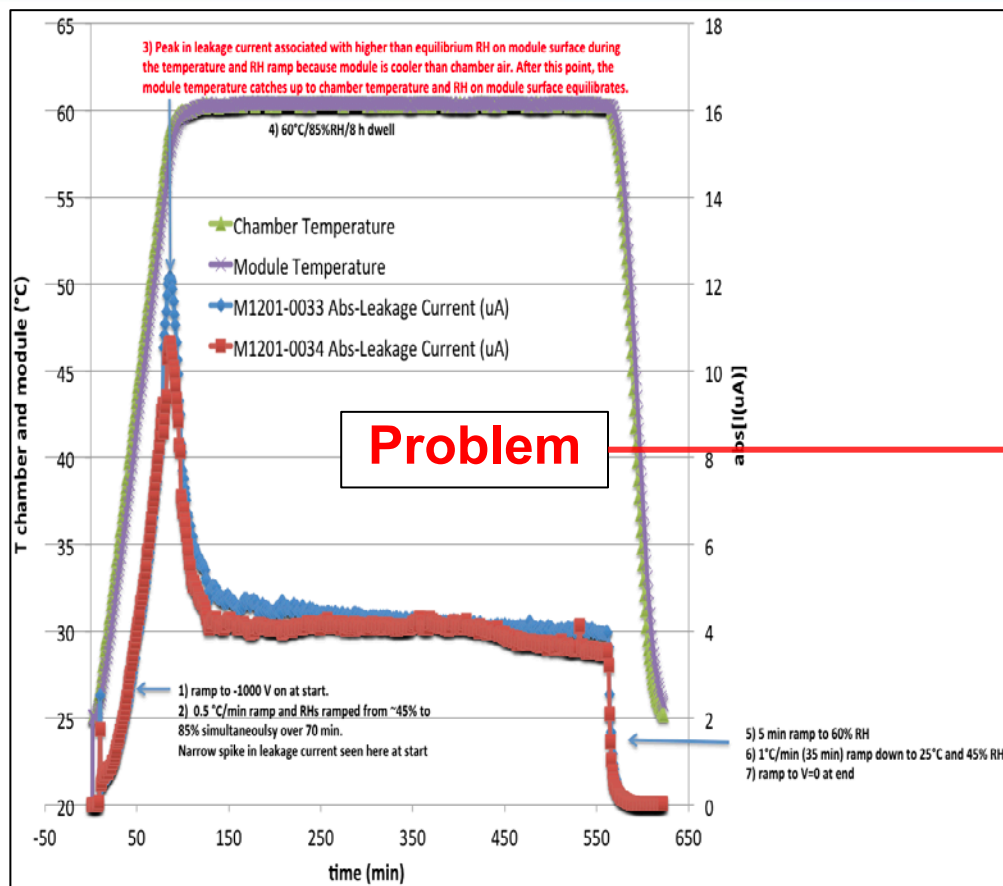
PID: Dependence on temperature and humidity



Temperature Level:

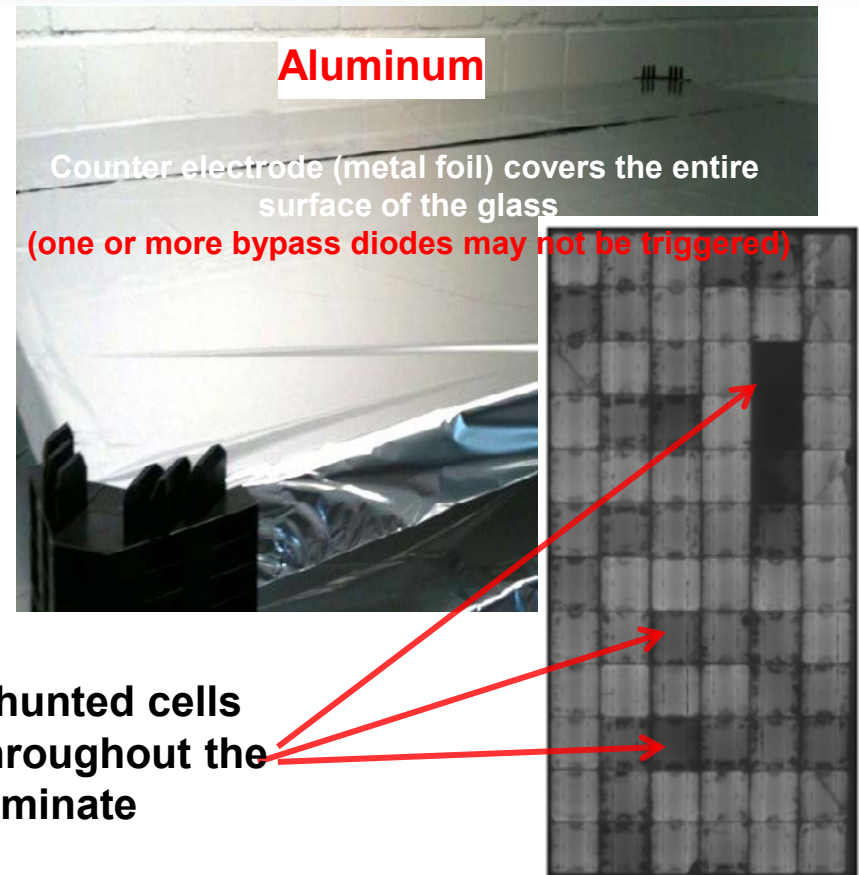
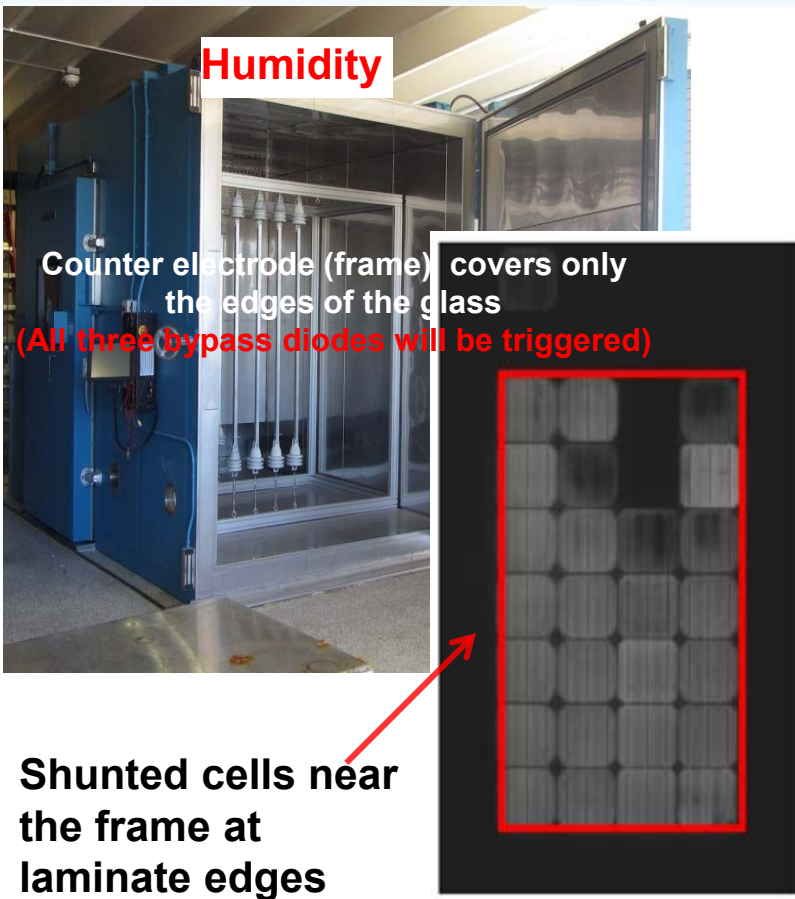
85°C stress temperature degrades silicon nitride and increases series resistance which are not observed in the field (reduce the temperature to 60°C)

PID: Dependence on temperature, humidity and voltage ramp sequence



Temperature, Humidity & Voltage Ramp Sequence:
Apply temperature, humidity and voltage ramps sequentially as shown above

PID: Dependence on counter electrode (frame) location



Counter Electrode Location:
Humidity method seems to better replicate the field degradation pattern as compared to the aluminum method (see slide 10)

PID: IEC Standard (Draft)

Standard: Problem, Test Development & Reproducibility

- **Problem**

- Current IEC 61215 and IEC 61646 qualification standards do not include the PID stress test.

- **Standardized Test Development**

- Based on the experience gained from the field tests and accelerated tests, develop an accelerated PID qualification test to replicate the field failure mechanism (junction shunting) and pattern (near the frame) in the shortest time possible.

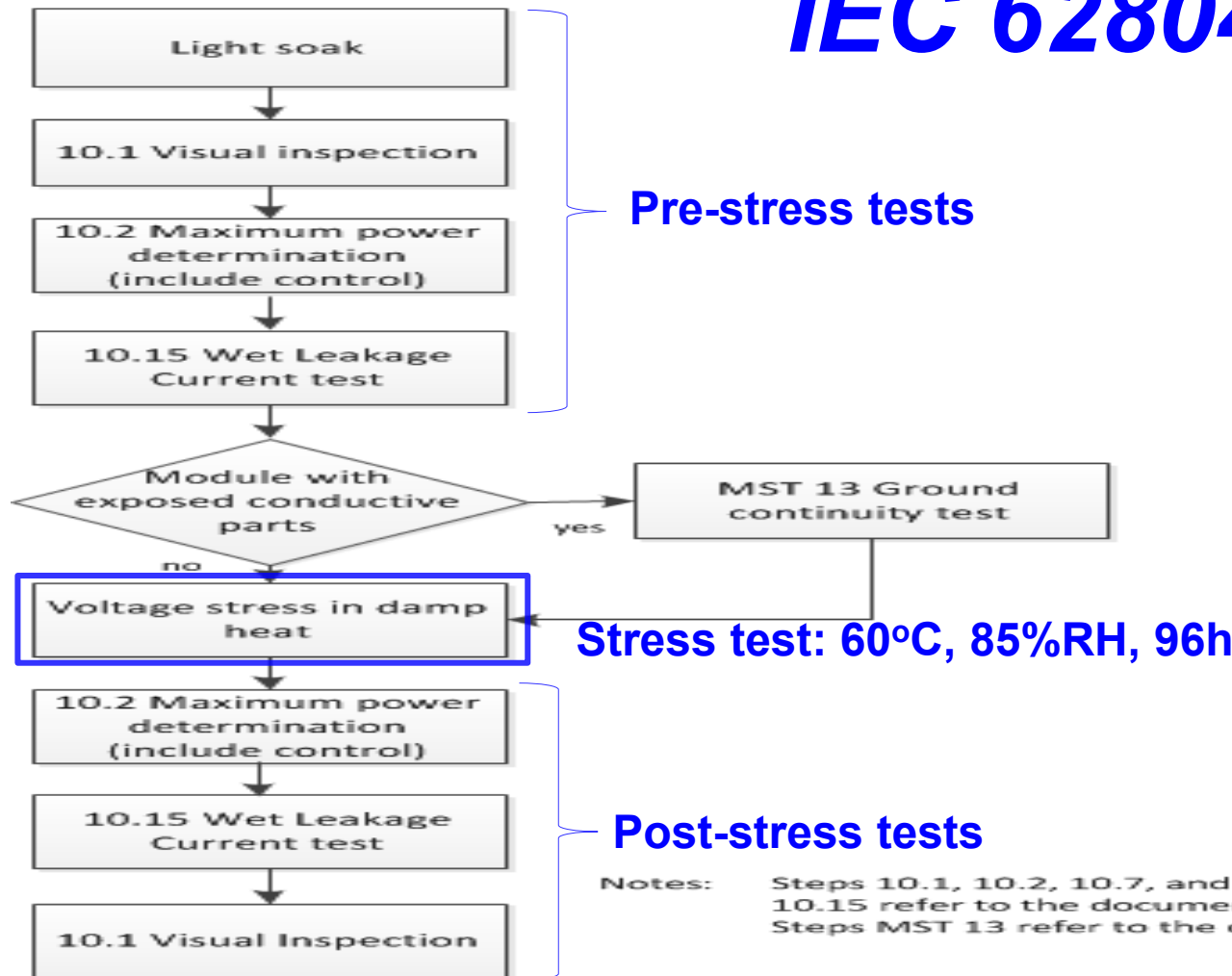
- **Reproducibility**

- Ensure that the accelerated qualification test results are reproducible between the test labs around the world so the results obtained from different labs are acceptable to the stakeholders.

Standard: Test Development

IEC 62804 Draft

Two modules per polarity



Notes: Steps 10.1, 10.2, 10.7, and 10.15 refer to the document IEC 61215 ed.2.0
Steps MST 13 refer to the document IEC 61730-2 ed.1.0

Standard: Test Development and Pass Criteria

a. Modules shall be exposed to the following stress test conditions:

- a. Chamber air temperature: 60 °C ± 1°C*
- b. Chamber relative humidity: 85 % ± 3 % RH
- c. Test duration: 96 h dwell at above stated temperature and relative humidity,
- d. Voltage: module rated system voltage and polarities are applied to the shorted module leads and the module frame or mounting points.

b. Test Procedure

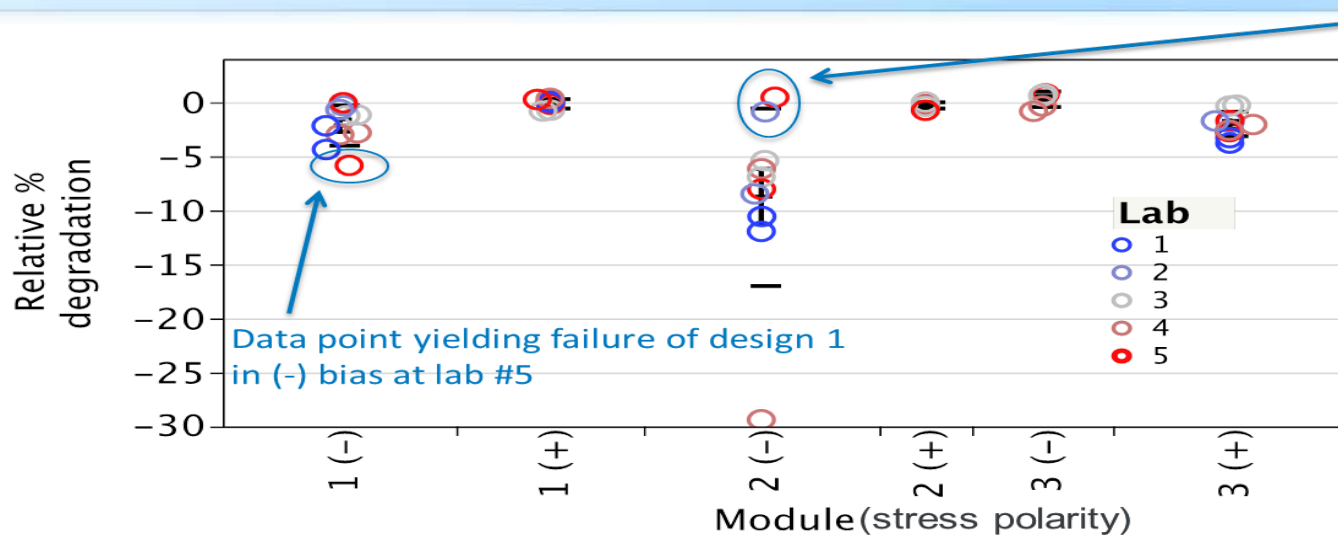
- i. The modules shall be at temperature before relative humidity is ramped. Voltage shall then be applied to the prescribed stress level.
- ii. The testing shall reasonably accommodate mounting instructions of the module manufacturer to simulate manufacturer-specified mounting configuration and conditions of the module in the least favorable extremes of the natural environment while ensuring the stress levels and factors specified here are maintained.

c. Pass/Fail Criteria

- i. The Standard Test Condition maximum power < 5% degradation (or just report degradation %?)
- ii. No major visual defects (IEC 61215 Ed. 2 Clause 10.1),
- iii. Wet leakage current test (IEC 61215 Ed. 2. Clause 10.15) results meet all requirements initially and after stress testing.

* NOTE: "The temperature tolerance specified in this presentation is +/-1°C which may be challenging requirement to achieve in a few existing environmental chambers; this tolerance may have to be increased to +/-2°C but it is emphasized, as per IEC 60068-2-78, that achieving fluctuations less than 0.5°C is recommended to maintain the specified RH% within tolerance. The RH and temperature tolerance specifications of this presentation will be superseded by the IEC 62804 standard when published".

Standard: Reproducibility Validation by Round Robin Testing



As anticipated, design 2 exhibited the greatest mean degradation and standard deviation in the susceptible polarity.

What is the probability of both those 2 modules that degraded less than 5% arriving at one lab, and thus passing the stress test in the (-) polarity at that one lab? ... There are 45 different combinations when the number of samples is 10 with 2 samples in each combination. The probability of those two ending up at one lab for a false pass is 1/45 (2.22%).

Participants				
Lab name	Level	Number	Mean	Std Dev
NREL	1 (-)	10	-2.12	1.87
Fraunhofer ISE	1 (+)	8	-0.10	0.43
TÜV Rheinland	2 (-)	10	-8.70	8.22
Fraunhofer CSP	2 (+)	4	-0.29	0.32
PI Berlin	3 (-)	6	0.30	0.68
	3 (+)	10	-1.99	1.13

Pass/fail criterion: If one or both modules tested in a polarity fail (P_{\max} drop > 5%), that design is considered failed in that polarity at the given test lab

Consistent pass/fail results, except for one design with mean degradation -2.12% relative that failed at one lab. The largest variability is attributed to variability within the module design. Based on this round robin testing, the RH tolerance is now tightened from +/-5% to +/-3%.

PID: Conclusions

Conclusions

▪ Critical significance of PID

- PID can cause very large degradation, so should not be ignored
- PID can be detected with a relatively short test

▪ Field Observations and Accelerated Test Results

- Degradation dependence is dictated by the module/cell type
- Degradation dependence is dictated by the bias level and polarity
- Degradation rate is very sensitive to temperature and humidity level and variability
- Cell degradation pattern within a module depends on the counter electrode location

▪ IEC Standard (Draft)

- Chamber air temperature: $60\text{ °C} \pm 1\text{ °C}^*$
- Chamber relative humidity: $85\% \pm 3\% \text{ RH}$
- Test duration: 96 h

▪ Round Robin Testing for Reproducibility Validation

- The largest variability between the test labs is attributed to variability within the module design. Based on the recent round robin testing, the RH tolerance is now tightened from $\pm 5\%$ to $\pm 3\%$.

Thanks for Your Attention!

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Additional Information

Standard: Voltage Stress in Dry Environment (Under Consideration)

Sunny-side

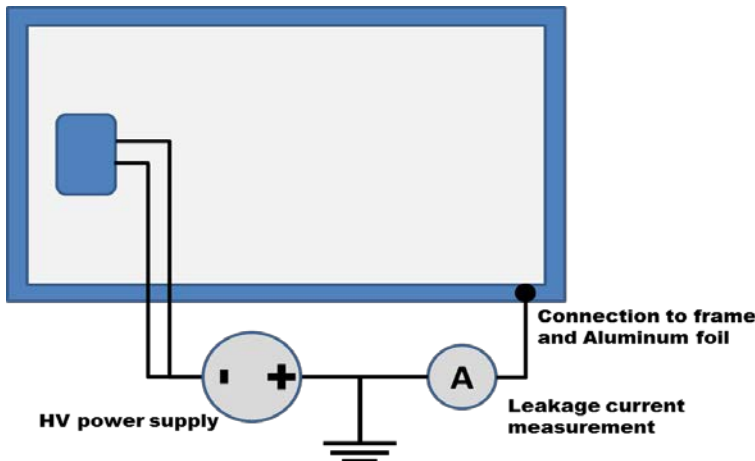
Al-foil

Frame

Tape

Tape

Conductive foil placement on module's surface and fixing on the frame



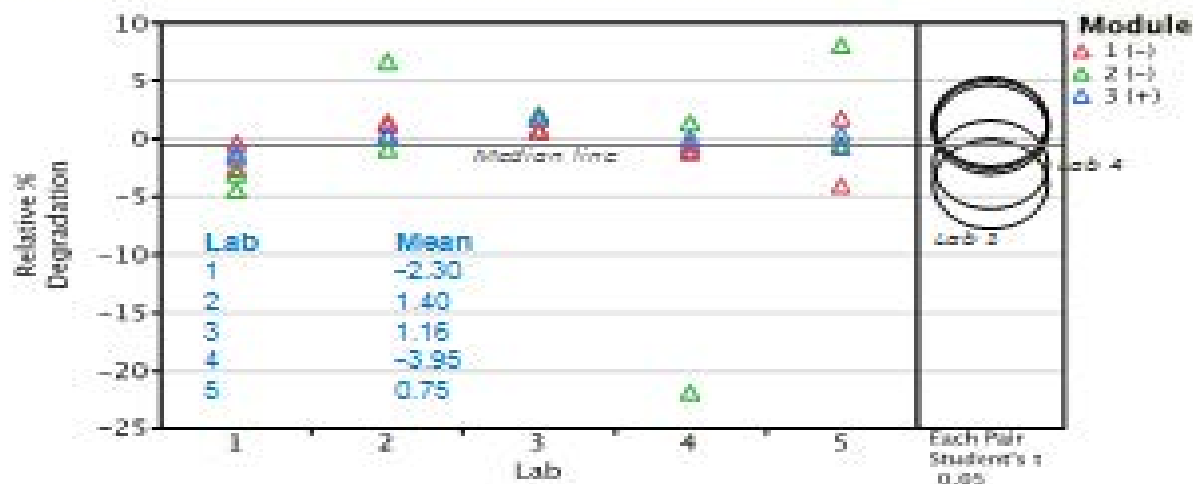
Schematic wiring for the voltage stress test - one polarity

The following conditions shall be applied:

- Chamber air temperature $25\text{ }^{\circ}\text{C} \pm 1\text{ }^{\circ}\text{C}$,
- PV module surface and edges are covered with a conductive foil (e.g. Aluminum foil) as shown in the adjacent figures
- Test durations 168h and 504h
- Voltage: module rated system voltage and polarities. Voltage ramp rate: max. 500 V/s. End of ramp defines start of test time

Standard: Reproducibility Validation by Round Robin Testing

Examination of lab-to-lab variability



Subtracting median degradation for each module type in this analysis failed to show a statistical significance in difference between labs.

Degradation may be more pronounced in labs 1 and 4. More uniformity in the results from lab to lab may be obtained by:

- Tightening of the temperature and relative humidity tolerances
- Application of voltage bias stress after modules have reached equilibrium conditions in the environmental chamber